

In the Claims:

Claims 1-14 are canceled, new claims 15-29 are added.

1. (canceled)
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14. (canceled)

15. (new) A vector graphics circuit arrangement for rendering vector and bitmap graphics objects to a final image, adapted to be associated in operation with a control processing unit arranged for decomposing graphics objects in Bézier curves edges, comprising:

display list memory adapted for receiving an input stream of object data from the said control process unit, the input stream of object data including at least an edge data sequence representative of Bézier curve edges of the graphics objects stored into the display list in ordered mode with Y increasing;

a Bézier hardware decomposing circuit for vector curve subdivision, coupled to said display list memory means and arranged for dividing Bézier curves into a series of subsegments and storing them into an active edge table,

said Bézier hardware circuit comprising a subdivision Bézier parameter unit, comprising a predetermined plurality of couples of adders/divide by two units, arranged for calculating the X and Y coordinates representing the anchor and control points of each Bézier curve subsegment; and

a sorting hardware circuit coupled to said display list memory as well as to said Bézier hardware decomposing circuit, and adapted for implementing a raster scan conversion algorithm of the Bézier curve edges, including:

an X-sorter circuit arranged to sort the edges parameters of a current scan line, read in the active edge table, with increasing X values, and

an active edge processor for storing the edge parameters of a current scan line sorted by the X-sorter circuit inside the active edge table, at an address generated by a free active edge address LIFO stack,

wherein both the X-sorter circuit and the active edge table comprise a dual port memory including two alternating ping-pong buffers.

16. (new) A vector graphics circuit arrangement according to claim 15, further comprising an antialiasing hardware circuit arranged for calculating the values of a predetermined number of subpixels present in a real display pixel, and for determining a weight factor for a scan-converted row.

17. (new) A vector graphics circuit arrangement according to claim 16, further comprising a color hardware circuit arranged for acceding to a plurality of bitmaps and mathematical tables stored inside the display list memory means.

18. (new) A vector graphics circuit arrangement according to claim 16, further comprising a dump buffer hardware circuit arranged for composing the vector graphics objects in a final color pixel bitmap.

19. (new) A vector graphics circuit arrangement according to claim 17, further comprising a dump buffer hardware circuit arranged for composing the vector graphics objects in a final color pixel bitmap.

20. (new) A vector graphics circuit arrangement according to claim 16, wherein the predetermined number of subpixels in a real display pixel is defined as  $N = i * 4$ , where  $i$  represents the number of simultaneously processed pixels per clock, which is less or equal the number of pixel in a row.

21. (new) A vector graphics circuit arrangement according to claim 17, wherein the color hardware circuit includes:

a. a color generator subunit arranged for outputting a solid or a processed color when a linear gradient, a radial gradient, a tiled bitmap or a clipped bitmap are associated with the active edge; and

b. a color composer subunit arranged for using the weight factor to process the color from the color generator and store the result in to a dump hardware buffer circuit;

wherein the color composer subunit reduces the number of memory accesses to the plurality of bitmaps and mathematical tables by the times of repetitions of the transformed destination pixel in to the dump hardware buffer circuit.

22. (new) A vector graphics circuit arrangement according to claim 18, further comprising a dump buffer hardware circuit

arranged for composing the vector graphics objects in a final color pixel bitmap.

23. (new) A vector graphics circuit arrangement according to claim 15, further comprising a color hardware circuit arranged for acceding to a plurality of bitmaps and mathematical tables stored inside the display list memory means.

24. (new) A vector graphics circuit arrangement according to claim 23, further comprising a dump buffer hardware circuit arranged for composing the vector graphics objects in a final color pixel bitmap.

25. (new) A vector graphics circuit arrangement according to claim 23, wherein the color hardware circuit includes:

a. a color generator subunit arranged for outputting a solid or a processed color when a linear gradient, a radial gradient, a tiled bitmap or a clipped bitmap are associated with the active edge; and

b. a color composer subunit arranged for using the weight factor to process the color from the color generator and store the result in to a dump hardware buffer circuit;

wherein the color composer subunit reduces the number of memory accesses to the plurality of bitmaps and mathematical tables by the times of repetitions of the transformed destination pixel in to the dump hardware buffer circuit.

26. (new) A vector graphics circuit arrangement according to claim 24, wherein the dump buffer hardware circuit is adapted to store a pixel region into a buffer, where all the objects are composed, comprising:

a. a fixed single line dump hardware buffer circuit memory adapted to store the color pixels processed by antialiasing and transparenance factors;

b. a store buffer memory adapted to store the color pixel bitmap value using the following algorithm:

i. Reading the background pixel from a store buffer memory, multiplying it by the complementary of the transparenance, obtained from the dump buffer hardware circuit, and adding it with the red, green, blue values of the output color from the color generator sub unit;

ii. writing the result again inside the store buffer memory;

wherein the dump buffer hardware circuit does not required the control process unit to resend the input stream of object data if the pixel region is modified.

27. (new) A vector graphics circuit arrangement according to claim 19, wherein the dump buffer hardware circuit is adapted to store a pixel region into a buffer, where all the objects are composed, comprising:

a. a fixed single line dump hardware buffer circuit memory adapted to store the color pixels processed by antialiasing and transparence factors;

b. a store buffer memory adapted to store the color pixel bitmap value using the following algorithm:

i. Reading the background pixel from a store buffer memory, multiplying it by the complementary of the transparence, obtained from the dump buffer hardware circuit, and adding it with the red, green, blue values of the output color from the color generator sub unit;

ii. writing the result again inside the store buffer memory;

wherein the dump buffer hardware circuit does not required the control process unit to resend the input stream of object data if the pixel region is modified.

28. (new) A vector graphics circuit arrangement according to claim 15, further comprising a dump buffer hardware circuit arranged for composing the vector graphics objects in a final color pixel bitmap.

29. (new) A vector graphics circuit arrangement according to claim 28, wherein the dump buffer hardware circuit is adapted to store a pixel region into a buffer, where all the objects are composed, comprising:

a. a fixed single line dump hardware buffer circuit memory adapted to store the color pixels processed by antialiasing and transparenance factors;

b. a store buffer memory adapted to store the color pixel bitmap value using the following algorithm:

i. Reading the background pixel from a store buffer memory, multiplying it by the complementary of the transparenance, obtained from the dump buffer hardware circuit, and adding it with the red, green, blue values of the output color from the color generator sub unit;

ii. writing the result again inside the store buffer memory;

wherein the dump buffer hardware circuit does not required the control process unit to resend the input stream of object data if the pixel region is modified.